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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,398	09/24/2001	Masaki Kurasawa	011254	5650

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EXAMINER

LE, THAO X

ART UNIT PAPER NUMBER

2814

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/960,398

Applicant(s)

KURASAWA ET AL.

Examiner

Thao X Le

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 15-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Group I claims 1-14 in Paper No. 6 is acknowledged.

### ***Drawings***

2. Figure 19A-C, 20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP0200028696 to Hiyama et al. in view of US 5,998,236 to Roeder et al.

Regarding to claim 1, Hiyama discloses a capacitor comprising: a buffer structure 3 formed on a substrate 1, a lower electrode 4, and formed of a perovskite ferroelectric material 5, having a crystal oriented substantially perpendicular to a surface of the lower electrode, and an upper electrode 6 formed on the capacitor dielectric film.

But Hiyama does not expressly disclose the perovskite ferroelectric material having a smaller thermal expansion coefficient (CTE) than that of the buffer structure.

However, Roeder reference discloses the substrate material of MgO has CTE larger than the CTE of PZT, column 2 lines 21-23. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the CeO<sub>2</sub> buffer structure 3 of Hiyama with the MgO teaching of Roeder, because it would have been able to control the orientation of the crystal lattice structure of ferroelectric film, column 2 lines 10-11.

Regarding to claim 2, Hiyama discloses the silicon substrate 1 and PZT capacitor dielectric 5; therefore the CTE of PZT would be larger than that of the silicon substrate.

Regarding to claim 3, as discussed in the claims 1 and 2 above; Hiyama and Roeder disclose all the limitations in claim 3.

Regarding to claim 4, Hiyama discloses the platinum (Pt) lower electrode 4 and PZT capacitor dielectric 5; therefore the CTE of Pt metal would be larger than that of the PZT.

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Regarding to claims 5, 7, 9 and 11, Hiyama discloses the capacitor wherein the capacitor dielectric film 5 has (001) oriented tetragonal and (111) oriented rhombohedral crystal structure, see abstract.

Regarding to claims 6, 8, 10 and 12, Hiyama discloses the capacitor wherein the lower electrode 4 has (100) and (111) cubic oriented crystal structure, see abstract.

5. Claim 13<sup>-14</sup> is rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub. 2002/0063274 to Kanaya et al. in view of US 5,998,236 to Roeder et al.

Regarding to claim 13, Kanaya discloses a semiconductor device in fig. 4B comprising: a memory cell transistor 10 formed on a semiconductor substrate 1, and including a gate electrode 12, and source/drain diffused layers 13/14 formed in the semiconductor substrate respectively on both sides of the gate electrode, an insulating film 2a/2b covering the semiconductor substrate with the memory cell transistor formed on, a buffer structure 3a, fig. 3f, formed on the insulation film, a capacitor 20 on the buffer structure, and including a lower electrode 3b, fig. 3f, electrically connected to one of the source/drain diffused layers, a capacitor dielectric film formed 4a formed on the lower electrode, and formed of a perovskite ferroelectric material 4a, having a crystal oriented substantially perpendicular to a surface of the lower electrode fig. 5 [0094], and an upper electrode 6 formed on the capacitor dielectric film.

But Kanaya does not expressly disclose the perovskite ferroelectric material having a smaller CTE than that of the buffer structure.

However, Roeder reference discloses the substrate material of MgO has CTE larger than the CTE of PZT, column 2 lines 21-23. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the buffer

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layer 3a of Kanaya with MgO layer of Roeder, because it would have been able to control the orientation of the crystal lattice structure of ferroelectric film, column 2 lines 10-11.

Regarding to claim 14, Kanaya discloses a semiconductor device in fig. 4B comprising: a memory cell transistor 10 formed on a semiconductor substrate 1, and including a gate electrode 12, and source/drain diffused layers 13/14 formed in the semiconductor substrate respectively on both sides of the gate electrode, an insulating film 2a/2b covering the semiconductor substrate with the memory cell transistor formed on, a buffer structure 3a, fig. 3f, formed on the insulation film, a capacitor 20 formed on the insulation film, and including a lower electrode 3b,fig. 3f, electrically connected to one of the source/drain diffused layers, a capacitor dielectric film 4a formed on the lower electrode, and formed of a perovskite ferroelectric material 4a, having a crystal oriented substantially perpendicular to a surface of the lower electrode fig. 5 [0094], and an upper electrode 6 formed on the capacitor dielectric film.

But Kanaya does not expressly disclose the CTE of perovskite ferroelectric material having a larger CTE than that of the substrate.

However, Kanaya discloses the silicon substrate 1 and PZT capacitor dielectric 5; therefore the CTE of PZT would be larger than that of the silicon substrate.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. US 5719417

b. US 6194818

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- c. US 6258459
- d. US 2001/0015448
- e. US 6265230
- f. US 6156623
- g. US 6136639
- h. US 2001/0002708
- i. US 5889299

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-T from 7:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le  
August 7, 2002

  
PHAT X. CAO  
PRIMARY EXAMINER